What is claimed is:

1. A method of accessing memory comprising:

accessing a first pair of adjacent data blocks using a first channel of a dual channel memory device; and

simultaneously accessing a second pair of adjacent data blocks using a second channel of the memory device, the second pair being spaced apart from the first pair by a predetermined interval.

2. The method of Claim 1, wherein the adjacent data blocks of the first pair have adjacent address values.

3. The method of Claim 1, wherein the data blocks each consist of a fixed number of bytes and the first block of the first pair is spaced apart from the first block of the second block by eight times the fixed number.

4. The method of Claim 1, further comprising providing the accessed data blocks to a graphics controller.

5. The method of Claim 1, further comprising receiving data blocks from a graphics controller and wherein accessing the data blocks comprises writing the received data blocks to the memory device.

6. The method of Claim 1, wherein the memory device is a double data rate memory device.

7. A machine-readable medium having stored thereon data representing instructions which, when executed by a machine, cause the machine to perform operations comprising:

accessing a first pair of adjacent data blocks using a first channel of a dual channel memory device; and

simultaneously accessing a second pair of adjacent data blocks using a second channel of the memory device, the second pair being spaced apart from the first pair by a predetermined interval.

8. The medium of Claim 7, wherein the adjacent data blocks of the first pair have adjacent address values.

9. The medium of Claim 7, wherein the data blocks each consist of a fixed number of bytes and the first block of the first pair is spaced apart from the first block of the second block by eight times the fixed number.

10. The medium of Claim 7, further comprising providing the accessed data blocks to a graphics controller.

11. A memory map for interleaved memory comprising:

a first channel having a first sequence of pairs of consecutive data blocks; and

a second channel having a second sequence of pairs of consecutive data blocks, the pairs of the first sequence alternating in sequential order with the pairs of the second sequence.

12. The memory map of Claim 11, wherein the first sequence of pairs consists of odd pairs and the second sequence consists of even pairs.

13. The memory map of Claim 11, wherein the data blocks are numbered sequentially, wherein the first sequence of pairs comprises a pair of blocks 0,1 and a pair of blocks 4 and 5, and wherein the second sequence of pairs comprises a pair of blocks 2 and 3 and a pair of blocks 6 and 7.

14. The memory map of Claim 11, wherein the first and second sequences of pairs have a transition interval and wherein after each occurrence of the interval the first and second sequences reverse order.

15. The memory map of Claim 14, wherein the first sequence of pairs consists of odd pairs before the first transition point and the second sequence consists of even pairs, and wherein the first sequence consists of even pairs after the first transition interval and before a second transition interval, and wherein the second sequence consists of odd pairs after the first transition interval and before the second transition interval.

16. The memory map of Claim 14, wherein the first and second sequences are chosen to optimize memory access speed by a selected controller.

17. The memory map of Claim 16, wherein the controller is a graphics processor.

18. A method of mapping memory comprising:

mapping a first pair of data blocks to a first channel of a dual channel memory;

mapping a second pair of data blocks to a second channel of the dual channel memory;

mapping a third pair of data blocks to the first channel of the dual channel memory;

mapping a fourth pair of data blocks to the second channel of the dual channel memory;

mapping a fifth pair of data blocks to the second channel of the dual channel memory; and

mapping a sixth pair of data blocks to the first channel of the dual channel memory.

19. The memory map of Claim 18, wherein the data blocks each comprise a quadword.

20. The memory map of Claim 19, wherein each pair of data blocks consists of two sequential quadwords.

21. The memory map of Claim 20, wherein the first, second, third and fourth pairs combined contain of 64 bytes.

22. A method of configuring a memory map comprising:

detecting devices coupled to a memory controller; and

selecting a primary device from among the detected devices for memory access; and

selecting a system memory memory map to optimize system memory operation with the selected device.

23. The method of Claim 22, wherein detecting devices comprises detecting a processor and a graphics controller.

24. The method of Claim 22, wherein selecting a primary device comprises determining a memory configuration for a detected graphics controller.

25. The method of Claim 22, wherein selecting a primary device comprises selecting a processor if a detected graphics controller includes internal memory and selecting the graphics controller if the graphics controller uses system memory.

26. The method of Claim 22, wherein selecting a memory map comprises selecting a system memory map to optimize graphics memory access if the graphics controller is selected.

27. A machine-readable medium having stored thereon data representing instructions which, when executed by a machine, cause the machine to perform operations comprising:

detecting devices coupled to a memory controller; and

selecting a primary device from among the detected devices for memory access; and

selecting a system memory memory map to optimize system memory operation with the selected device.

28. The medium of Claim 27, wherein detecting devices comprises detecting a processor and a graphics controller.

29. The medium of Claim 27, wherein selecting a primary device comprises

30. A computer system comprising:

a graphics controller;

a dual channel memory;

a central processing unit; and

a memory controller coupled by a bus to the CPU, the dual channel memory and the graphics controller, the memory controller having a memory map to the first channel of the dual channel memory having a first sequence of pairs of consecutive data blocks, and memory map to the second channel of the dual channel memory having a second sequence of pairs of consecutive data blocks,

the pairs of the first sequence alternating in sequential order with the pairs of the second sequence.

31. The system of Claim 30, wherein the first and second sequences of pairs have a transition interval and wherein after each occurrence of the interval the first and second sequences reverse order.

32. The system of Claim 30, wherein the first sequence of pairs consists of odd pairs before the first transition point and the second sequence consists of even pairs, and wherein the first sequence consists of even pairs after the first transition interval and before a second transition interval, and wherein the second sequence consists of odd pairs after the first transition interval and before the second transition interval.